IN THE CLAIMS

1. (Currently Amended) A data transmission device comprising:

a clock generation circuit generating a clock signal;

a jitter generator ~~supply circuit allowing~~ generating jitter in the clock signal ~~generated by the clock generation circuit to include jitter~~ based on a setting signal; and

a data transmission circuit transmitting data in sync with the clock signal including the jitter.

2. (Currently Amended) The data transmission device according to claim 1, wherein

the jitter generator ~~supply circuit~~ adjusts [[the]] an amount of modulation or [[and/or]] the frequency of the jitter ~~included in the clock signal~~.

3. (Currently Amended) The data transmission device according to claim 1, wherein

the jitter generator ~~supply circuit~~ generates ~~supplies, as the jitter,~~ at least [[any]] one of a sinusoidal jitter and a random jitter in the clock signal.

4. (Currently Amended) The data transmission device according to claim 2, wherein

the jitter generator supply circuit generates ~~supplies, as the jitter,~~ at least [[any]] one of a sinusoidal jitter and a random jitter in the clock signal.

5. (Currently Amended) An I/O interface circuit comprising:

a clock generation circuit generating a first clock signal;

a jitter generator ~~supply circuit allowing~~ generating jitter in the first clock signal ~~generated by the clock generation circuit to include jitter~~ based on a setting signal; and

a data transmission circuit transmitting data in sync with the first clock signal including the jitter.

6. (Currently Amended) The I/O interface circuit according to claim 5, wherein

the jitter generator ~~supply circuit~~ adjusts [[the]] an amount of modulation or [[and/or]] the frequency of the jitter ~~included in the first clock signal~~.

7. (Currently Amended) The I/O interface circuit according to claim 5, wherein

the jitter generator ~~supply circuit~~ generates ~~supplies, as the jitter,~~ at least [[any]] one of a sinusoidal jitter and a random jitter in the first clock signal.

8. (Currently Amended) The I/O interface circuit according to claim 6, wherein

the jitter generator ~~supply circuit~~ generates ~~supplies, as the jitter,~~ at least [[any]] one of a sinusoidal jitter and a random jitter in the first clock signal.

9. (Currently Amended) The I/O interface circuit according to claim 5, further comprising:

a data reception circuit receiving data, wherein

the clock generation circuit also supplies a second clock signal to the data reception circuit,

the data transmission circuit comprises: ~~includes~~

pattern generation circuit generating a data pattern for a jitter resistance test, and

transmission circuit allowing the data pattern generated by the pattern generation circuit to be transmitted in sync with the first clock signal, and

the data reception circuit comprise: ~~includes~~

reception circuit allowing the data pattern received by the transmission circuit to be received in sync with the second clock signal, and

pattern comparison circuit comparing the data pattern received by the reception circuit with an expectation value to output a comparison result.

10. (Currently Amended) The I/O interface circuit according to claim 9, further comprising

measurement result storage circuit associatively storing the comparison result delivered by the pattern comparison circuit and information on [[the]] an amount of modulation or [[and/or]] the frequency of the jitter ~~supplied by the jitter supply circuit~~.

11. (Currently Amended) The I/O interface circuit according to claim 9, further comprising:

a jitter generator ~~supply circuit~~ control circuit controlling the jitter generator ~~supply circuit~~ to vary the amount of modulation and/or the frequency of the jitter in accordance with the comparison result delivered by the pattern comparison circuit and a measurement procedure for the jitter resistance.

12. (Currently Amended) The I/O interface circuit according to claim 9, wherein

the jitter generator ~~supply circuit~~ control circuit controls the jitter generator ~~supply circuit~~ so as to vary the amount of modulation of the jitter when the comparison result delivered by the pattern comparison circuit indicates a match and to vary ~~whereas varying~~ the frequency of the jitter when the comparison result delivered by the pattern comparison circuit indicates a mismatch.

13. (Currently Amended) The I/O interface circuit according to claim 9, wherein

the pattern generation circuit in the data transmission circuit further comprises:

a circuit ~~function~~ including data of a contiguous sequence of 0s or 1s in the data pattern, and

the pattern comparison circuit in the data reception circuit further comprises ~~comprising~~:

a first circuit ~~function~~ detecting the data of a contiguous sequence of 0s or 1s having been received, and

a second circuit ~~function~~ forcing the comparison result to indicate a match when the first circuit ~~function~~ detects the data of a contiguous sequence of 0s or 1s having been received.

14. (Original) The I/O interface circuit according to claim 13, wherein

the pattern generation circuit in the data transmission circuit replaces part of the data pattern with data of a contiguous sequence of 0s or 1s, thereby allowing the data pattern to include the data of a contiguous sequence of 0s or 1s.

15. (Original) The I/O interface circuit according to claim 13, wherein

the pattern generation circuit in the data transmission circuit inserts data of a contiguous sequence of 0s or 1s into a midpoint of the data pattern, thereby allowing the data pattern to include the data of a contiguous sequence of 0s or 1s.

16. (Currently Amended) The I/O interface circuit according to claim 13, wherein

the pattern generation circuit in the data transmission circuit further comprises a circuit ~~function~~ adjusting a cycle in a case of data of a contiguous sequence of 0s or 1s being included in the data pattern in that cycle.

17. (New) The data transmission device according to claim 1, further comprising:

a selector selecting the clock signal including the jitter based on a control signal.

18. (New) The data transmission device according to claim 1, further comprising:

a first voltage controlled oscillator receiving the clock signal including the jitter; and

a second voltage controlled oscillator.

19. (New) The I/O interface circuit according to claim 5, further comprising:

a selector selecting the first clock signal including the jitter based on a control signal.

20. (New) The I/O interface circuit according to claim 5, further comprising:

a first voltage controlled oscillator receiving the first clock signal including the jitter; and

a second voltage controlled oscillator.